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EXAMINER	
TSAI, H JEY	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/710,272	Applicant(s) DORIS ET AL.	
	Examiner H.Jey Tsai	Art Unit 2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,10-15 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,10-15 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6, 10-15, 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hareland et al. 6,909,151, in view of Sugii et al. 2004/0108559, previously applied.

The reference discloses:

Hareland et al. discloses a method of forming an electronic device, comprising:

forming at least one localized stressor region (stress incorporating layer formed above of beneath the channel region, such as silicon nitride layer 360 or 560 or oxide layer 319 or Cobalt silicide 430, same material as instant invention) within the device, col. 2, lines 33-67, col. 6, line 28-67, figs. 3-4,

forming a second localized stressor region within the device (layer 360 formed above or beneath or cobalt silicide layer 430 on each source/drain or layer 319 beneath the channel region), fig. 3A, 3B, 4, col. 2, lines 33-67, col. 6, line 28-67, figs. 3-5,

first localized stressor region and said second localized stressor region causing a channel region to be stressed, col. 2, lines 33-67, col. 6, line 28-67, col.13, lines 1-56, figs. 3-5,

first localized stress-stressor region and said second localized comprise a same type material of SiN or oxide or cobalt silicide, col. 7, lines 1-25, col. 13, lines 1-55,

the same type material comprises one of a compressive stressor material and a, tensile stressor material, col. 2, line 45-57, col. 6, lines 58-67,col. 7, lines 1-25, col. 13, lines 1-55,

device is a FinFET (Fin Field Effect Transistor), fig. 4-5,

forming fin connector 520 to connect the FinFETs and forming a stressor 560, 430, fig. 5E and col. 10, lines 13-67,

first and second localized stressor regions are formed on a source and drain region 430 of the FinFET, fig. 4,

device comprises a planar FET (Field Effect Transistor), fig. 1, 2A,

comprises a compressive carriers in said region being stressed the same type material and primary charge comprise holes (carriers), col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55,col, 7, lines 20-67, col. 13, lines 31-55,

the same type material comprises a tensile material and primary charge carriers in the region being stressed comprise electrons (carriers), col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55.

The region being stressed causes carrier mobility in the stressed region into one of increased and decreased, relative to a carrier mobility in a region without the stress, col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55,

forming a blocking mask, col. 10, lines 36 col. 12, line 35,

at least one of localized stressor region 360 or 560 or 430 interacts with a stressed region located outside said device, fig. 3A, 3B, 5C,

wherein said at least one localized stressor is used to generate one of a compressive and a tensile stress, col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55,

wherein the at least one localized stressor region is located within the device to generate a Stress that enhances a performance of the device, col. 2, lines 33-57, col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55,

wherein the enhancement comprises an increase in performance enhancement by changing carrier mobility, col. 2, lines 33-57, col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55,

wherein at least one localized stressor region 360 or 560 is located to generate a stressed region in at least one of a direction parallel to a current flow and perpendicular to a current flow, (stressor formed on top only or side only or bottom only),

wherein at least one localized stressor region 360 or 560 or silicide is used to create a symetrically stressed region (formed on top and bottom),

wherein at least one localized stressor region 360 or 560 or silicide is used to create an asymmetrically stressed region (stressor formed on top only or side only or bottom only).

The difference between the reference(s) and the claims are as follows: Hareland et al. teaches forming localized stressor layer on the source/drain region but does not clearly show that source/drain region is a part connector. However, Sugii et al. teaches

at figs. 13-14, 19-29, para. 123-153, the source/drain regions 4 is a part of fin connector and forming localized stressor 5 on the of the fin connector 4. Sugii et al. also teaches forming a localized stressor 5 on the channel region, See figs. 13-14, 19-29.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used source/drain regions as a fin connector as taught by Sugii et al. because fin connector can be formed as same time as source/drain regions.

Claims 1-4, 6, 10-15, 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hareland et al. 6,909,151, in view of Matsumoto et al. 2004/0227185 or Kumagai et al. 2004/0075148 or Ke et al. 2005/0079677, all are previously cited.

The reference discloses:

Hareland et al. discloses a method of forming an electronic device, comprising:

forming at least one localized stressor region (stress incorporating layer formed above of beneath the channel region, such as silicon nitride layer 360 or 560 or oxide layer 319 or Cobalt silicide 430, same material as instant invention) within the device, col. 2, lines 33-67, col. 6, line 28-67, figs. 3-4,

forming a second localized stressor region within the device (layer 360 formed above or beneath or cobalt silicide layer 430 on each source/drain or layer 319 beneath the channel region), fig. 3A, 3B, 4, col. 2, lines 33-67, col. 6, line 28-67, figs. 3-5,

first localized stressor region and said second localized stressor region causing a channel region to be stressed, col. 2, lines 33-67, col. 6, line 28-67, col.13, lines 1-56, figs. 3-5,

first localized stress-stressor region and said second localized comprise a same type material of SiN or oxide or cobalt silicide, col. 7, lines 1-25, col. 13, lines 1-55,

the same type material comprises one of a compressive stressor material and a, tensile stressor material, col. 2, line 45-57, col. 6, lines 58-67,col. 7, lines 1-25, col. 13, lines 1-55,

device is a FinFET (Fin Field Effect Transistor), fig. 4-5,

forming fin connector 520 and source/drain regions at same time to connect the FinFETs and forming a stressor 560, 430, fig. 5B, 5E and col. 10, lines 13-67, col. 6, lines 15-27,

first and second localized stressor regions are formed on a source and drain region 430 of the FinFET, fig. 4,

device comprises a planar FET (Field Effect Transistor), fig. 1, 2A,

comprises a compressive carriers in said region being stressed the same type material and primary charge comprise holes (carriers), col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55,col, 7, lines 20-67, col. 13, lines 31-55,

the same type material comprises a tensile material and primary charge carriers in the region being stressed comprise electrons (carriers), col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55.

The region being stressed causes carrier mobility in the stressed region into one of increased and decreased, relative to a carrier mobility in a region without the stress, col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55,

forming a blocking mask, col. 10, lines 36 col. 12, line 35,

at least one of localized stressor region 360 or 560 or 430 interacts with a stressed region located outside said device, fig. 3A, 3B, 5C,

wherein said at least one localized stressor is used to generate one of a compressive and a tensile stress, col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55,

wherein the at least one localized stressor region is located within the device to generate a Stress that enhances a performance of the device, col. 2, lines 33-57, col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55,

wherein the enhancement comprises an increase in performance enhancement by changing carrier mobility, col. 2, lines 33-57, col. 6, lines 30-35, col, 7, lines 20-67, col. 13, lines 31-55,

wherein at least one localized stressor region 360 or 560 is located to generate a stressed region in at least one of a direction parallel to a current flow and perpendicular to a current flow, (stressor formed on top only or side only or bottom only),

wherein at least one localized stressor region 360 or 560 or silicide is used to create a symetrically stressed region (formed on top and bottom),

wherein at least one localized stressor region 360 or 560 or silicide is used to create an asymmetrically stressed region (stressor formed on top only or side only or bottom only).

The difference between the reference(s) and the claims are as follows: Hareland et al. teaches forming a fin connector in figs. 5B, 3A, and source/drain regions is a part of fin connector (see col. 6, line 15-27), forming localized silicide layer 430 on the

source/drain region but does not teach that cobalt silicide layer having high stress property. However, Matsumoto et al. para. 39 and 80, fig. 19, that cobalt silicide formed as a localized stressor 13 by increasing the stresses in the channel region of the transistor. Kumagai et al. teaches at para. 208-210 and fig. 16, forming a cobalt silicide layer 181, 381 on the source/drain regions as a localized stressor. Ke et al. teaches at para. 23, 31, 33, figs. 5-7, forming localized silicide stressors 708, 709 and dielectric stressors 702a, 702b., 706a, 706b.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized that cobalt silicide increases the stresses in the channel region of the transistor as suggested by Matsumoto et al. or Kumagai et al. or Ke et al. because the stresses enhanced the carrier mobility of the transistor.

Claims 1-4, 6, 10-15, 23-30 are rejected under 35 U.S.C 103 as being unpatentable over Yeo et al. 2004/0173815, in view of Sugii et al. 2004/0108559, previously applied.

Yeo et al. discloses a method of forming an electronic device, comprising:

forming at least one localized stressor region 305a within the device, para. 30-34, 8-15, figs. 3A-3B, or figs. 4A-11D, para. 35-64,

forming a second localized stressor region 305b within the device fig. 2A-2B,

first localized stressor region and said second localized stressor region causing a channel region to be stressed, para. 30-34, 8-15 or figs. 4A-11D, para. 35-64,

first localized stress-stressor region and said second localized comprise a same type material silicon germanium or silicon carbide, para. 30-34, 8-15 or figs. 4A-11D, para. 35-64,

the same type material comprises one of a compressive stressor material and a,

tensile stressor material, para. 30-34, 8-15 or figs. 4A-11D, para. 35-64,

device comprises a planar FET (Field Effect Transistor), fig. 3A,

comprises a compressive carriers in said region being stressed the same type material and primary charge comprise holes (carriers), para. 30-34, 8-15 or figs. 4A-11D, para. 35-64,

the same type material comprises a tensile material and primary charge carriers in the region being stressed comprise electrons (carriers), para. 30-34, 8-15 or figs. 4A-11D, para. 35-64,

the region being stressed causes carrier mobility in the stressed region into one of increased and decreased, relative to a carrier mobility in a region without the stress, para. 30-34, 8-15 or figs. 4A-11D, para. 35-64,

at least one of localized stressor region 305a, 305b interacts with a stressed region located outside said device, fig. 3A-3B, 8-15 or figs. 4A-11D, para. 35-64,

wherein said at least one localized stressor is used to generate one of a compressive and a tensile stress, para. 30-34, 8-15 or figs. 4A-11D, para. 35-64,

wherein the at least one localized stressor region is located within the device to generate a Stress that enhances a performance of the device, para. 30-34, 8-15 or figs. 4A-11D, para. 35-64,

wherein the enhancement comprises an increase in performance enhancement by changing carrier mobility, para. 30-34, 8-15 or figs. 4A-11D, para. 35-64,

wherein at least one localized stressor region is located to generate a stressed region in at least one of a direction parallel to a current flow and perpendicular to a current flow, figs. 3A-3B, para. 30-34, 8-15 or figs. 4A-11D, para. 35-64,

wherein at least one localized stressor region 3051, 305b or silicide is used to create a symetrically stressed region, para. 30-34, 8-15 or figs. 4A-11D, para. 35-64.

The difference between the references applied above and the instant claim(s) is: Yeo et al. teaches forming localized stressors in the source/drain regions but does not teach forming localized stressor in a FinFET device. However, Sugii et al. teaches at figs. 13-14, 19-29, para. 123-153, the source/drain regions 4 is a part of fin connector and forming localized stressor 5 on the fin connector 4. Sugii et al. also teaches forming a localized stressor 5 on the channel region, See figs. 13-14, 19-29.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by forming localized stressors in the source/drain fin connector regions of the FinFET device as taught by Sugii et al. because localized stressors formed in the source/drain regions would induces stresses in the channel region to enhanced the carrier mobility (current) for better device performance.

Claims 1-4, 6, 10-15, 23-30 are rejected under 35 U.S.C 103 as being unpatentable over Chen et al. 2005/0190421, in view of Sugii et al. 2004/0108559, previously applied.

Chen et al. discloses a method of forming an electronic device, comprising:

forming at least one localized stressor region 911 within the device, para. 44-45, 36. fig. 9,

forming a second localized stressor region 913 within the device fig. 9,

first localized stressor region and said second localized stressor region causing a channel region to be stressed, para. 44-45,

first localized stress-stressor region and said second localized comprise a same type material silicide, para. 36. 44-45,

the same type material comprises one of a compressive stressor material and a,

tensile stressor material, para. 44-45,

comprises a compressive carriers in said region being stressed the same type material and primary charge comprise holes (current), para. 44-45,

the same type material comprises a tensile material and primary charge carriers in the region being stressed comprise electrons (current), para. 44-45,

the region being stressed causes carrier mobility (current) in the stressed region into one of increased and decreased, relative to a carrier mobility in a region without the stress, para. 44-45,

at least one of localized stressor region 911, 193 interacts with a stressed region located outside said device, fig. 9, para. 44-45,

wherein said at least one localized stressor is used to generate one of a compressive and a tensile stress, para. 44-45,

wherein the at least one localized stressor region is located within the device to generate a stress that enhances a performance of the device, para. 44-45,

wherein the enhancement comprises an increase in performance enhancement by changing carrier mobility (current), para. 44-45,

wherein at least one localized stressor region is located to generate a stressed region in at least one of a direction parallel to a current flow and perpendicular to a current flow, fig, 9, para. 44-45,

wherein at least one localized stressor region 911, 913 or silicide is used to create a symmetrically stressed region, para. 44-45, fig. 9.

The difference between the references applied above and the instant claim(s) is: Chen et al. teaches forming localized stressors in the source/drain regions but does not teach forming localized stressor in a FinFET device. However, Sugii et al. teaches at figs. 13-14, 19-29, para. 123-153, the source/drain regions 4 is a part of fin connector and forming localized stressor 5 on the fin connector 4. Sugii et al. also teaches forming a localized stressor 5 on the channel region, See figs. 13-14, 19-29.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by forming localized stressors in the source/drain regions of the FinFET device as taught by Sugii et al. because localized stressors formed in the source/drain regions would induces stresses

in the channel region to enhanced the carrier mobility (current) for better device performance.

Conclusions

Applicant's arguments filed May 27, 2008 have been fully considered but they are not persuasive. Because newly cited references Sugii et al. clearly teaches in figs. 13-14, 19-29 and para. 123-153, a first localized stressor/strain 5 formed on the right-hand sidewall of the fin connector region 4 and a second localized stressor/strain 5 formed on the left-hand sidewall of the fin connector 4. For example in figs. 24-27C and 28-29C, the strain/stress layer 5 is formed on the sidewall of the fin connector 4 (see fig. 25C, 26C, 29C).

FIG.24

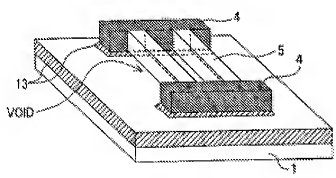


FIG.25A

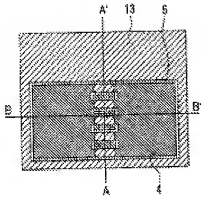


FIG.25B

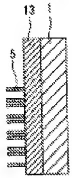


FIG.25C

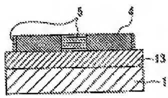


FIG.26A

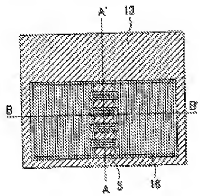


FIG.26B

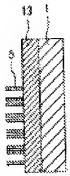


FIG.26C

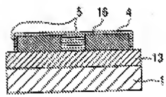


FIG.28

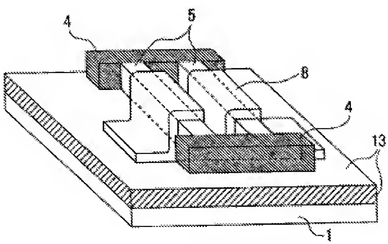


FIG.29A

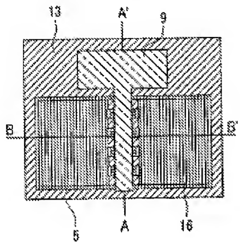


FIG.29B

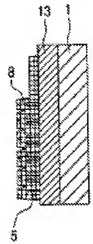
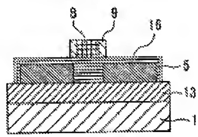


FIG.29C



And, Hareland et al. clearly teach forming a localized stressor 430 in the source/drain regions. The source/drain region is a part of fin connector, see col. 6, lines 15-27, fig. 3A, 5B. And, Hareland also clearly teaches forming at least one localized stressor region (stress incorporating layer formed above of beneath the channel region, such as silicon nitride layer 360 or 560 or oxide layer 319 or Cobalt silicide 430, same material as instant invention) within the device, figs. 3-4, forming a second localized stressor region within the device (layer 360 formed above or beneath or cobalt silicide

layer 430 on each source/drain or layer 19 beneath the channel region), first localized stressor region and said second localized stressor region causing a channel region to be stressed as set forth above. Hareland et al. clearly teaches the meaning of localized stressor that meets the claimed invention at figs.3-4 and col. 6, lines 36-46, a localized stressor layer 360 embedded in the tri-gate FinFET device 300 by depositing around the exposed portion of semiconductor body (fin connector part, see fig. 3A) 308, over and around the gate electrode 324 as well as directly on or adjacent to the sides 310, 312 of semiconductor body 308. Since, device 300 is a tri-gate FinFET transistor (including three gate electrodes and 3 pairs of source/drain regions), hence localized stressor layer 360 is clearly localized within the tri-gate FinFET device 300 and causing a channel region 350 to be stressed (see col. 2, lines 33-67, col. 6, lines 28-67, col. 13, lines 1-56 and figs. 3-5 as set forth in the last Final rejection). Hareland teaches at col. 8, lines 8-20, isolated locallized silicide stressor 430 also can be formed on the fin connector region 308 (see col. 8, lines 42-55), an isolated stressor 319 and/or localized stressor 360 formed on the fin connection region (connection part) 308, 520 (see col. 8, lines 42-65, col. 10, lines 13-67, fig. 5E of Hareland. Silicide film stressor 450/430 can form a localized stressor on top of gate electrode 324, 325 see col. 8, lines 56-65 of Hareland.

Since, Hareland teaches forming cobalt silicide layer on the source/drain regions, and Metsumoto or Kumagai or Ke teaches cobalt silicide as stressor in source/drain regions, hence the combination of Hareland and Metsumoto or Kumagai or Ke is proper. Therefore, it is clearly that the combination of Hareland and Metsumoto or

Kumagai or Ke meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of “a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability”. And, it is also clearly that the combination of Hareland and Metsumoto or Kumagai or Ke meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of “If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103”.

Since, Yeo et al. teaches forming localized stressor on the source/drain regions, and Sugii teaches forming a localized stressor in source/drain regions of fin connectors, hence the combination of Yeo and Sugii is proper. Therefore, it is clearly that the combination of Yeo and Sugii meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of “a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability”. And, it is also clearly that the combination of Yeo and Sugii meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of “If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103”.

Since, Chen et al. teaches forming localized stressor on the source/drain regions, and Sugii teaches forming a localized stressor in source/drain regions of fin connectors, hence the combination of Chen and Sugii is proper. Therefore, it is clearly that the combination of Chen and Sugii meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of “a person of ordinary skill can implement a predictable

variation, §103 likely bars its patentability". And, it is also clearly that the combination of Chen and Sugii meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of "If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103".

And, specific dimension of stressor, such as localized stressor as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating suchconcentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable rangesby routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955), see MPEP § 2144.04 (obvious range).

In Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative

dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

It is well settled that where patentability is predicated upon a change in a condition of a prior art feature, such as a change in size, concentration, or the like, the burden is on the applicant to establish with objective evidence that the change is critical, i.e., it leads to a new, unexpected result. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990); In reAller, 220 F.2d 454, 456, 105 USPQ 233,235 (CCPA 1955). See MPEP 2144.04 § IV.

More details of U.S. Supreme Court in KSR international v. Teleflex, US Supreme Court, 127 S.Ct. 1727 (2007): Granting patent protection to advances that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known elements, deprive prior inventions of their value or utility. When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103.

When a work is available in one field, design incentives and other market forces can prompt variations of it, either in the same field or in another. If a person of ordinary skill in the art can implement a predictable variation, and would see the benefit of doing so, §103 likely bars its patentability. Moreover, if a technique has

been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill.

It is common sense that familiar items may have obvious uses beyond their primary purposes, and a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle. See KSR international v. Teleflex, US Supreme Court, 127 S.Ct. 1727 (2007).

In *Sakraida* v. *AG Pro, Inc.*, 425 U. S. 273(1976), the Court derived from the precedents the conclusion that when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious. *Id.*, at 282. The principles underlying these cases are instructive when the question is whether a patent claiming the combination of elements of prior art is obvious. When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736.

The fax phone number for this Group is 571-273-8300.

/H.Jey Tsai/
Primary Examiner, Art Unit 2895